REMARKS

Claim 1 has been amended above for clarification purposes. No new matter has been added.

Claims 1 to 9 and 18 are now pending. Applicants respectfully request reconsideration of the present application in view of this response.

Claims 1 to 3, 5 to 8, and 18 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,222,108 to Suzuki ("Suzuki reference").

Applicants respectfully submit that the Suzuki reference does not identically describe or suggest each and every feature of the claims, as required for anticipation. Specifically, the Suzuki reference recites a cell transmission phase and rate converting circuit for use in an ATM communication system in which an internal write-in pulse generator generates an internal write-in pulse sequence having a predetermined write-in period on the basis of each cell phase pulse of an external write-in pulse sequence. The Suzuki reference recites using a control unit for controlling an FIFO buffer to write a write-in cell data into the FIFO buffer as held cell data in response to a write-in clock signal and the internal write-in pulse sequence and to read the held cell data out of the FIFO buffer as read-out cell data in response to a read-out clock signal and the internal read-out pulse sequence.

In contrast, claim 1 of the present invention concerns a device for receiving data transmitted using asynchronous data transmission technology, the device including a data-independent clock signal and a memory device, and *storing the received data for the required period of time in order to compensate for transmission delays*. In the claimed invention, the independent data clock signal is sent to the memory device for readout of the data. The Suzuki reference does not identically describe that such a device stores the received data for the required period of time such that a period between two disturbances is made long that any effect of the two disturbances is reduced. Further, the Suzuki reference appears to teach away from the present invention of the use of a data-independent clock, i.e., the studio clock signal which is sent to the memory device for reading data, in that the Suzuki reference recites that using the control unit to initialize the buffer is "disadvantageous" because such initialization will cause the buffer to discard other cell data and the operation of the first and second ATM circuit stops during initialization. Accordingly, Applicants respectfully submit that claim 1 and its dependent claims 2 to 3, 5 to 8, and 18 are allowable. Applicants respectfully request withdrawal of the rejection under 35 U.S.C. § 102(b) of those claims.

Claims 4 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Suzuki reference. Claims 4 and 9 depend from claim 1, which, as discussed above, is believed allowable over the Suzuki reference. Accordingly, Applicants respectfully submit that claims 4 and 9 are allowable, and request withdrawal of the rejection under 35 U.S.C. §103(a) of those claims.

CONCLUSION

In view of the foregoing, it is believed that the rejection of the claims under 35 U.S.C. §§ 102(b), 103(a) has been overcome, and that claims 1 to 9 and 18 are allowable. It is therefore respectfully requested that the rejections be withdrawn, and that the present application issue as early as possible.

In efforts to further the prosecution, Applicants kindly reiterate their request for an interview with the Examiner to discuss the above application.

Respectfully submitted,

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